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# Using Pseudo-Random Binary Sequences to Stress Test Serial Digital Interfaces

Whitepaper



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## Introduction

In this whitepaper, PHABRIX discusses the use of pseudo-random binary sequences (PRBS - also referred to as pseudo-random bit sequences), along with bit-error rate tests (BERT – also referred to as bit-error ratio tests) to stress test serial digital interfaces. The purpose of any physical layer serial digital interface (PHY) is to transmit or receive data whilst preserving that data’s integrity. In practical systems the major cause of bit-errors is random noise. To stress test such systems, it is necessary to both generate a “noisy” bit stream and then analyse the output from the interface to determine the bit-error rate which represents the integrity of the data.

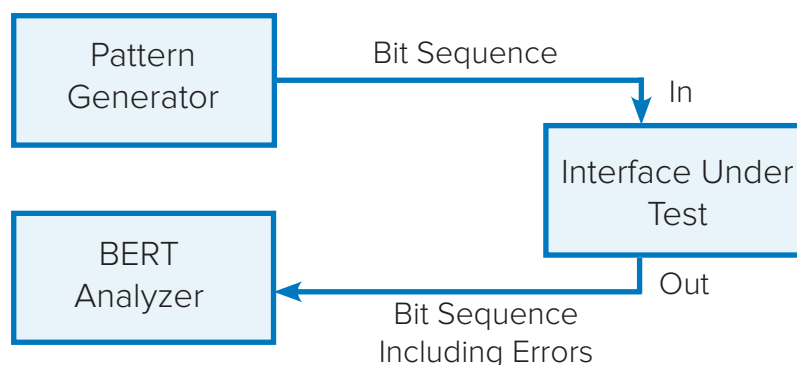
$$\text{Bit-Error Rate (BER)} = \frac{\text{Number of Bit-Errors}}{\text{Number of Bits Received}}$$

## What are PRBS sequences?

A PRBS sequence is a series of digital 1’s and 0’s that is statistically random within the sequence length. This type of sequence shows no correlation between adjacent bits and as such can be considered a “worst case” stress test signal for testing serial digital interfaces. If the interface can handle a “noisy” random sequence of bits without generating bit-errors, then we can be confident that it will be able to handle “clean” non-random sequences.

Although a PRBS sequence demonstrates random behaviour, it is in fact generated deterministically and the bit sequence will

always be the same when repeated. As an example, a PRBS7 sequence has a word length of 7-bits and will generate a sequence length of  $2^7 - 1$  (127) bits, which is repeated indefinitely by the pattern generator. In general, any PRBS $k$  sequence will have a word length of  $k$  bits and a sequence length of  $2^k - 1$  bits. It is this combination of both deterministic generation and random bit pattern that make these sequences ideal for testing interfaces. As the BERT analyser knows what PRBS bits were generated, it is relatively straight forward to conduct a bit-error count on the interface’s output bit stream.



## PRBS Pattern Generator and BERT Analyzer

## Which PRBS sequence should I use?

PRBS sequences can be generated using a range of sequence lengths. The PHABRIX Qx Stress Test toolkit offers PRBS7, 9, 15, 23 and 31. These range in sequence length from 127 bits (PRBS7) to 2,147,483,647 bits (PRBS31). The ITU-T 0.150 specification - general requirements for instrumentation for performance measurements on digital transmission equipment, makes the following recommendations for these sequences (see Table 1, below).

Running a PRBS sequence once, without repetition is unlikely to result in the generation of any bit-errors, so ideally the sequence should be repeated long enough to generate a minimum of 100 bit-errors. This will ensure that a statistically valid data sample provides an accurate bit-error rate measurement. With short sequence lengths, the pattern is repeated many times, which has the effect of reducing the randomness of the signal, especially at higher bit rates. Long sequence lengths offer more randomness, which stresses the interface more, leading to a higher likelihood of inducing bit-errors. However, they have the disadvantage of taking a longer time to complete the entire sequence, which can be a significant issue at lower bit rates.

As a result, it is generally recommended that short PRBS patterns be used at low bit rates

and long PRBS patterns be used at the highest bitrates. For SDI applications it is most common to use the PRBS23 sequence (8,388,607 bits). SDI interfaces may be designed to demonstrate bit-error rates of better than  $10^{-12}$  when stress tested in this way. With a target BER of  $10^{-12}$ , using a PRBS23 sequence to stress test a 3G SDI interface, we can expect one bit-error approximately every 5 to 6 minutes, which implies a total test time of around 9 hours to generate the desired 100 errors. To reduce test times, it may be acceptable to either reduce the number of detected errors below 100, or to test against higher BER target, perhaps better than  $10^{-10}$  for 3G SDI. For validation testing purposes, it is reasonable to test for better BER performance at higher bitrates, say better than  $10^{-11}$  for 12G and 6G interfaces and worse BER performance of say  $10^{-9}$  at SD bitrates.

Although, under stress test conditions, with a 3G SDI interface we may expect to generate one bit-error every 5 to 6 minutes (around 15,000 to 18,000 frames at 50 frames per second), under non-stress test operational conditions, we would expect to see no bit-errors (as indicated by CRC errors). SDI systems normally operate in an error-free environment and it is only under conditions of excessive jitter or noise that we may expect to see bit-errors.

Sequence	Length of Sequence	Length of Sequence (bits)	Use of Sequence	Comments
PRBS9	$2^9 - 1$	511	Error measurements on data circuits at bit rates up to 14,400 bit/s	PRBS-9 is one of the recommended test patterns for SFP+
PRBS15	$2^{15} - 1$	32,767	Error and jitter measurements at bit rates of 1544, 2048, 6312, 8448, 32,064 and 44,736 kbit/s	PRBS15 is often used for jitter measurement
PRBS23	$2^{23} - 1$	8,388,607	Error and jitter measurements at bit rates of 34,368 and 139,264 kbit/s	PRBS23 is one of the recommended test patterns for SDH/SONET  PRBS23 is also commonly used by SDI chip manufacturers to test interface performance
PRBS31	$2^{31} - 1$	2,147,483,647	Specific measurement tasks	PRBS31 is one of the recommended test patterns for 10 Gigabit Ethernet

Table 1

## How are PRBS sequences generated?

Hardware PRBS pattern generators are implemented using linear feedback shift registers (LFSR). In an LFSR the shift registers are arranged in series with a multi-tap feedback loop from the later stages back to the input of the 1st shift register. The feedback loop is implemented using exclusive OR/NOR gates. The number of shift registers determines the PRBS sequence length

and to implement a PRBS23 sequence, 23 stages are required, with taps from the outputs of the 23rd and 18th stages.

The required taps are represented using single-variable polynomials. For the PRBS sequences offered by the Qx Stress toolkit, these are as follows:

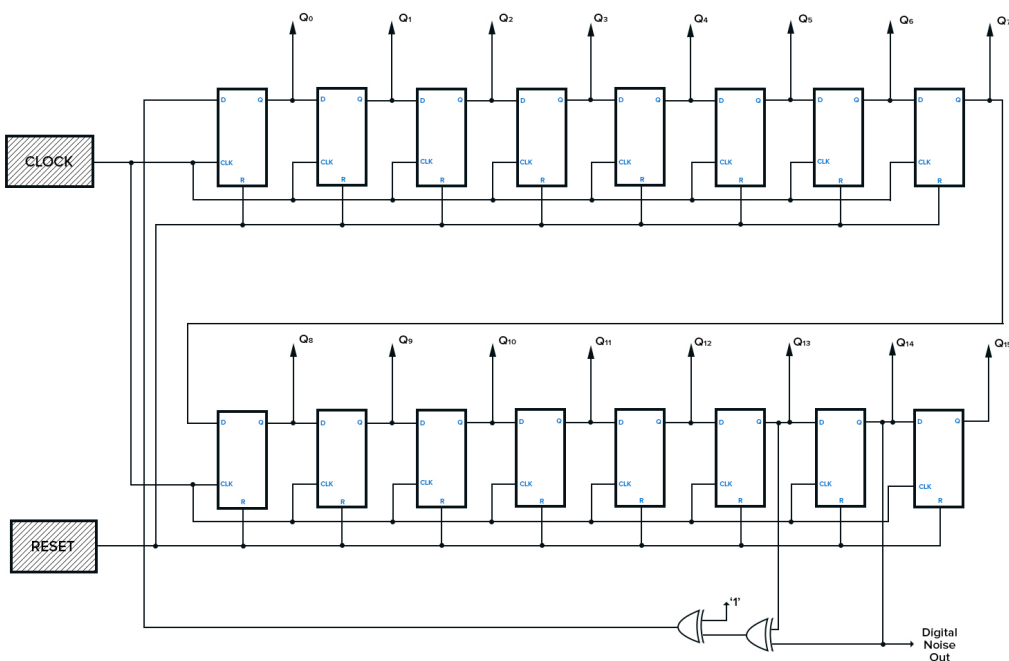
PRBS7 =  $x^7 + x^6 + 1$  (Taps from the 7th and 6th shift registers)

PRBS9 =  $x^9 + x^5 + 1$  (Taps from the 9th and 5th shift registers)

PRBS15 =  $x^{15} + x^{14} + 1$  (Taps from the 15th and 14th shift register)

PRBS23 =  $x^{23} + x^{18} + 1$  (Taps from the 23rd and 18th shift registers)

PRBS31 =  $x^{31} + x^{28} + 1$  (Taps from the 31st and 28th shift registers)



*Simplified PRBS15 Pattern Generator*

In the example shown above, note that only 15 of the 16 shift registers in the dual quad static shift register are used. The outputs from the 15th (Q14)

and 14th (Q13) shift registers are exclusive-ORed together, inverted and fed back to the 1st shift register.

	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>
Seed	1	1	1
1	0	1	1
2	0	0	1
3	1	0	0
4	0	1	0
5	1	0	1
6	1	1	0
7	1	1	1

### 3 Stage LFSR Data States

The exclusive OR example shown above, uses 3 shift registers with feedback taps from stages 3 and 2, to generate 7 ( $2^3 - 1$ ) possible states with at least one logic 1 bit. Note that the all 0s state is not allowable in the exclusive OR LFSR implementation and the all 1s state is not allowable in the exclusive NOR LFSR implementation. As a side note, linear feedback

shift registers are also used in the implementation of SDI scramblers, which are intended to avoid a long series of logic 1s or 0s appearing at the SDI interface. This is to minimise the DC component of the signal and to ensure that the signal reaching the receiver has a sufficiently large number of zero-crossings to permit reliable clock recovery.

## Using PRBS sequences for Eye Diagram testing

What is the best signal type to choose for eye diagram testing SDI interfaces – bars, zone plate, sports action, or something else? To answer that question, it is important to recognise that a properly constructed eye diagram consists of all possible combinations of 1's and 0's including isolated 0's and 1's after long runs of successive 1's and 0's. Any deviation from such a signal type will give different results for both vertical and horizontal Eye opening.

PRBS patterns are a suitable source of such pseudo-random combinations of 1's and 0's for eye diagram testing. Shorter PRBS word length patterns will give shorter runs of successive 1's and 0's (all 0's being illegal), so it is recommended that longer patterns such as PRBS15 and PRBS23 are used. The results of any test should state which pattern was used so the test can be repeated.

## Conclusion

PRBS sequences generate a “noise-like” signal, which is an industry-wide accepted method of generating bit-errors in serial digital interfaces such as SDI. They provide a more flexible and complete method of stress testing serial digital interfaces than the use of pathological signals and jitter insertion alone, although both PRBS and pathological signals have their application in qualifying interface performance. PRBS sequences are also a suitable signal type for eye diagram testing. As PRBS signals are compatible with non-broadcast specific test equipment, it is possible to obtain confirmation of test results using such general-purpose test equipment.

The PHABRIX Qx SDI STRESS toolkit provides a complete solution for the test and validation of SDI interfaces. The toolkit provides various PRBS patterns (PRBS7, 9, 15, 23 and 31) suitable for use with a wide-range of bitrates, along with a built-in BERT Analyser tool. In addition, the toolkit offers fast, automated 12G-SDI physical layer analysis employing RTE™ (Real-Time Eye) technology, to provide a comprehensive solution to SMPTE standard compliance verification of 12G/6G/3G/HD-SDI interfaces. Also included are control over eye amplitude (+/-10%), pre-emphasis, signal polarity, output mute, and SDI scrambler. These operate in conjunction with a video pattern generator to overlay SDI pathological signals and to insert SDI jitter (10Hz to 10MHz) into the signal, along with a pathological EQ/PLL condition detector with real time trigger over GPI out.



For more information about  
PHABRIX's SDI STRESS  
Toolset:

[www.phabrix.com](http://www.phabrix.com)

